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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	**PAPER NUMBER**
1765	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/787,460	KAJI ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/365,642.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: "KV" is referenced throughout the Specification. It is noted that "KV" is different from "KeV," which is recited in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 2, 6, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Narasimhan et al. (US 6,372,301).

As to claims 1, 2, and 6, Applicants' admitted prior art illustrates and teaches a method of forming a dual damascene by etching a low-k dielectric layer, then forming a barrier layer over the etched dielectric layer, and filling the etched layer with copper (see pages 1-5, Description of the Related Art).

Applicants' admitted prior art fails to teach after etching a low-k material, providing a copper barrier treatment to an etched surface of the low-k material by a surface reforming process performed to carbonize, nitride, bromize, form into boride, reduce, or form into amorphous the etched surface, or a combination thereof; the surface reforming process being performed by making ions accelerated by voltage or neutral particles obtained by diselectrifying the accelerated ions collide against the etched surface in either a same processing chamber as where the low-k material was etched or in a different processing chamber after being transferred thereto in vacuum, **in claim 1**;

wherein a surface reforming material is deposited on the etched surface before making said accelerated ions or said neutral particles obtained by diselectrifying said accelerated ions collide against the etched surface, **in claim 2**;

prior to filling copper, forming at once a copper barrier layer on the side wall portions and the plane portions of the created plug portion by a plasma process utilizing a gas plasma generated from a mixture including at least a rare gas and one of the

following gases; carbon atom-containing gas, nitrogen atom-containing gas, hydrogen atom-containing gas, bromine atom-containing gas, or boron atom-containing gas, **in claim 6**; and

wherein the copper barrier layer is formed to reach a depth of 3 nm to 50 nm, **in claim 10**.

Narasimhan teaches a method for improving adhesion of diffusion layer on low-k FSG or a halogen-doped silicon oxide layer (Abstract). A barrier film, such as tantalum nitride is deposited by sputtering argon and nitrogen gas on target **316** with an RF power source and DC bias (column 5, lines 23-24 and column 6, lines 1-9 and 15-36). The diffusion barrier layer has a thickness between 50 A and 200 A (i.e. 5 and 20 nm), (column 6, lines 8-9)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art by using Narasimhan's method of depositing a barrier layer onto a low-k dielectric for the purpose of preventing silicon into an overlying metal layer (column 6, lines 1-3).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' admitted prior art.

As to claims 4 and 5 Applicants' admitted prior art illustrates and teaches a method of forming a dual damascene by etching a low-k dielectric layer, then forming a barrier layer over the etched dielectric layer, and filling the etched layer with copper (see pages 1-5, Description of the Related Art). Hence, the above reads on,

A method for forming a conductive damascene structure by filling copper in a plug portion formed on an insulating film, the method comprising: prior to filling copper in the plug portion, forming the plug portion by a film forming process and an etching process that provide either little or no copper barrier property to side wall portions and plane portions defining inner walls of the plug portion, and then forming at once a copper barrier layer on the side wall portions and the plane portions of the created plug portion by a plasma process utilizing a gas plasma including a component that functions as a barrier against copper, **in claim 4**; and

A method for forming a conductive damascene structure by filling copper in a plug portion formed on an insulating film, the method comprising: prior to filling copper in the plug portion formed to have on its inner wall a two-step trench portion comprising a large cross-section and a small cross-section via a plane portion, forming the plug portion by a film forming process and an etching process that provide either little or no copper barrier property to side wall portions and the plane portions defining the inner walls of the plug portion, and then forming at once a copper barrier layer on the side wall portions and the plane portions of the created plug portion having little or no copper

barrier property by a plasma process utilizing a gas plasma including a component that functions as a barrier against copper, **in claim 5**.

Claim Rejections - 35 USC § 103

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Van Buskirk et al. (US 6,184,550 B1).

Applicants' admitted prior art fails to teach forming at once a copper barrier layer on the sidewall portions and the plane portions of the created plug portion by a plasma process utilizing a gas plasma generated from a mixture of rare gas and hydrocarbon gases.

Van Buskirk teaches, "Barrier layers according to the present invention may be made by reactive sputtering using N_2, CH_4 (or other reactive sources of N and C), CVD, or by nitridation, carbidation or ion implantation of preexisting metallic layers (column 6, lines 53-56 and column 3, lines 13-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicants' admitted prior art by forming a barrier layer as taught by Van Buskirk for the purpose of minimizing the resistivity of barrier layer, such as in Cu barrier layers, which take up a significant fraction of the cross-section of the conductor in ULSI metallization schemes, and providing a barrier layer that would result in an amorphous or nanocrystalline microstructure, which will improve barrier properties and facilitate reduced barrier thickness (column 6, lines 1-10).

8. Claims 8, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art as applied respectively to claims 4, 5, and 7 above in view of Narasimhan (US '301 B1).

Applicants' admitted prior art fails to teach wherein the copper barrier layer is formed to reach a depth of 3 nm to 50 nm, **in claims 8, 9, and 11**.

Narasimhan teaches a method for improving adhesion of diffusion layer on low-k FSG or a halogen-doped silicon oxide layer (Abstract). A barrier film, such as tantalum nitride is deposited by sputtering argon and nitrogen gas on target **316** with an RF power source and DC bias (column 5, lines 23-24 and column 6, lines 1-9 and 15-36). The diffusion barrier layer has a thickness between 50 A and 200 A (i.e. 5 and 20 nm), (column 6, lines 8-9)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art by using Narasimhan's method of depositing a barrier layer onto a low-k dielectric for the purpose of preventing silicon into an overlying metal layer (column 6, lines 1-3).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Narasimhan (US '301 B1) as applied to claim 1 above, and claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Narasimhan (US '301 B1), both further in view of Jeng (US 2002/0068432 A1).

Applicants' admitted prior art in view of Narasimhan fails to teach accelerating the generated ions by 1 keV to 50 keV.

Jeng teaches patterning a dual damascene and ion implanting a predetermined region of a dielectric layer with 20 to 100 keV [0025 and 0026], which reads on and encompasses accelerating the generated ions by 1 keV to 0 keV.

It would have been obvious to one having ordinary skill in the art at the time the invention was made of modify Applicants' admitted prior art in view of Narasimhan by using Jeng method of implanting ions for the purpose of raising the yield and quality of the process of forming damascene [0011 and 0012].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 1765

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August 2, 2007

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER